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ARL 400 Amp Silicon Carbide Power Module

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ABSTRACT

The need for improved electrical power conversion systems and components is being driven by requirements for higher efficiency, performance, and improved survivability and lethality capabilities on current and future Army platform power system. The U.S. Army Research Laboratory (ARL) has demonstrated a 1200 V, 400 A silicon carbide (SiC) power module based on a standard commercial design. This module uses large area SiC MOS-FETs and diodes and has been evaluated under varying temperatures, loads, and switching frequencies. Throughout the operating range, the module has demonstrated improved efficiency and thermal performance, and higher frequency operation, when compared with similarly rated silicon insulated gate bipolar transistor (IGBT) modules.

INTRODUCTION

The Army's need for increasing power density, improved capabilities, and increased efficiency of power conversion systems is driving the development of silicon carbide (SiC) materials technologies. Silicon carbide has the potential to provide improved reliability while operating at higher temperatures, with lower losses [1]. For the past 20 years the U.S. Army Research Laboratory (ARL) has been working to develop SiC power switches and during the past 6 years has been focused on creating doubly implanted Metal Oxide Semiconductor Field Effect Transistor (DMOS-FET) switches [2][3] This technology provides a normal off, voltage-controlled switch that power engineers prefer; however, reliable MOS-FET's have proven to be a challenge due to poor oxide quality. Recent breakthroughs in the fabrication of these devices have allowed the fabrication of 70 amp MOS-FETs. This paper describes the use of these MOS-FETs in the development of an all SiC 1.2 kV, 400 A dual MOSFET power module in a standard half-bridge configuration with integrated cooling. The performance of this module under varying load conditions is also addressed.

MODULE DESIGN

The module was designed and fabricated at ARL to replace a standard 400 A dual insulated gate bipolar transistor (IGBT) module in a half-bridge configuration (Figure 1) and was designed to operate at 100 °C using a 50% aqueous solution of propylene glycol (PGW50/50). The SiC devices were provided by Cree, Inc. and their development was made possible by support from ARL, the U.S. Air Force Research Laboratory, and DARPA. The module uses a low-profile liquid cooled heat sink designed and fabricated at ARL.

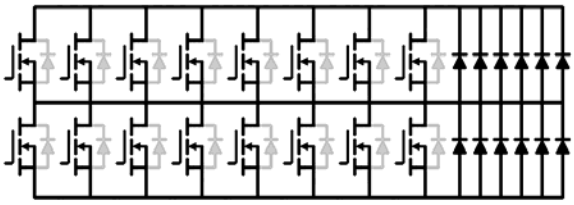

Figure 1 Electrical schematic of module

Design and layout of the circuit was optimized to reduce inductive losses, limit bond area, and simplify fabrication of the part while maintaining a commercially based dual IGBT package footprint [4]. To maintain drop in compatibility with the test bed and commercial systems a standard 62 mm x 107 mm dual IGBT/diode package was selected that is currently offered by component manufacturers in 300 to 450 A rated dual IGBT modules (Figure 2).

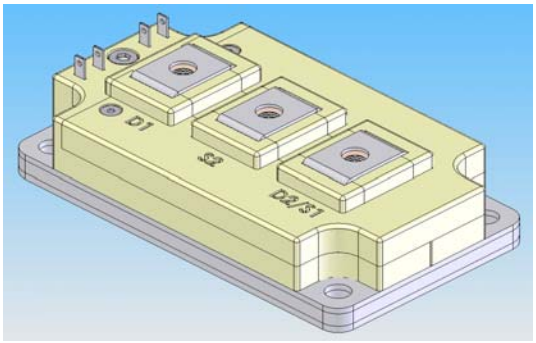

Figure 2 External module design

The devices were mounted to a patterned direct bond copper (DBC) substrate soldered directly to the heat sink. Reduction in inductive losses and bond area led to the use of four DBC substrates instead of a single larger one (Figure 3).

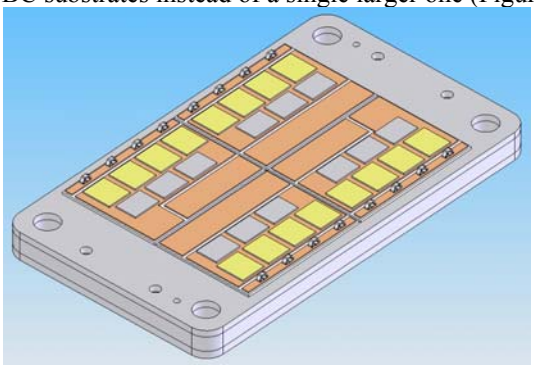

Figure 3 Quadrant layout of module

This technique did increase fabrication complexity by requiring two variant board designs. Each board contained eight Cree SiC MOS-FETs nominally rated at 50 A and 1200 V. Paired with the MOS-FETs are six CREE 1200 V Junction Barrier Sottkey diodes required for the half-bridge configuration. The devices were mounted to the DBC substrates using an 80Au-20Sn eutectic high temperature solder and the top surface connections were made with 12 mil aluminum wire [5]. The DBC substrates were bonded directly to the heat sink using a 96.5Sn-3.0Ag-0.5C solder and were interconnected using copper jumpers soldered to the substrate. External connections were made through copper terminals soldered to the substrates (Figure 4).

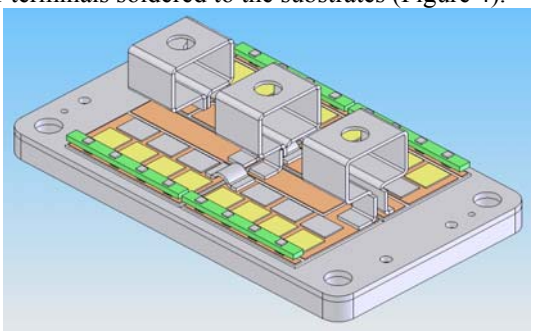

Figure 4 Terminal and jumper layout

Once all connection were made to the polysulfone plastic case, fabricated using a fused deposition modeling process, the holding gate terminals and fastening hardware were attached [5] (Figure 5). The case was designed to have a removable lid to allow thermal imaging of devices during testing.

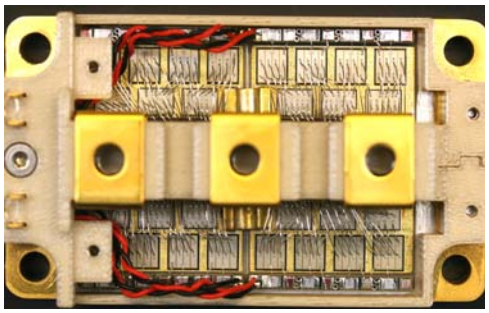

Figure 5 Completed module with lid removed

The heat sink was designed to provide high performance cooling in a low-profile design [6][7]. The design must have a low-pressure drop while maintaining the maximum device junction temperature below 175 °C at a 100 °C coolant temperature. Device-to-device temperature variations also had to be kept to a minimum. Fluid and thermal performance of the heat sink was extensively modeled to achieve these goals. The model used a per chip power dissipation of 86 W and simulated results were calculated at 1, 3, and 5 gpm. To reduce the pressure drop while maintaining high thermal performance, variations in channel flow were minimized (Figure 6) and the center was blocked to force coolant through the fins.

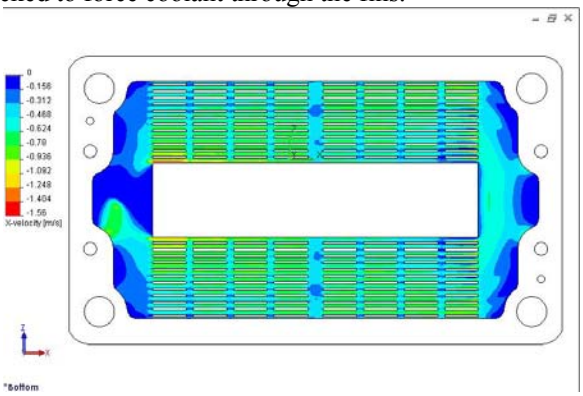

Figure 6 Flow fields through the heat sink

This also reduced device-to-device thermal variations (Figure 7).

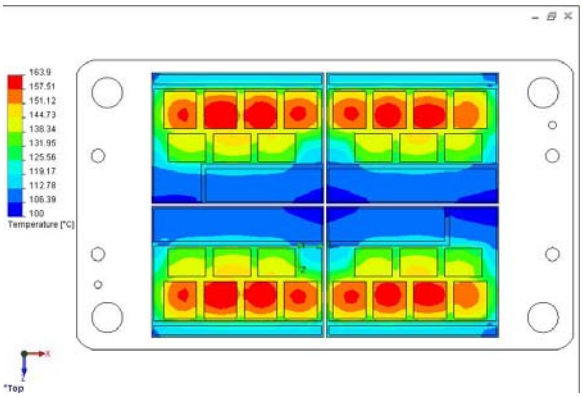

Figure 7 Modeled die temperature variations

This design provided a low profile heat sink that exceeded the performance goals (Table 1).

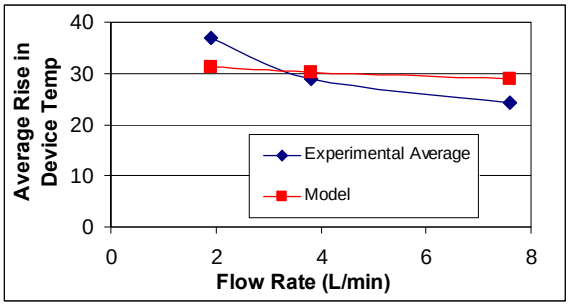

Table 1 Heat sink performance modeled versus experimental

The completed design was fabricated from a modified off-the-shelf finned copper heat sink soldered to a copper base plate (Figure 8 and Figure 9).

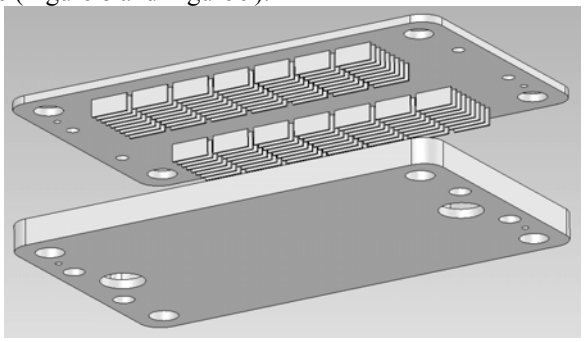

Figure 8 Heat sink design

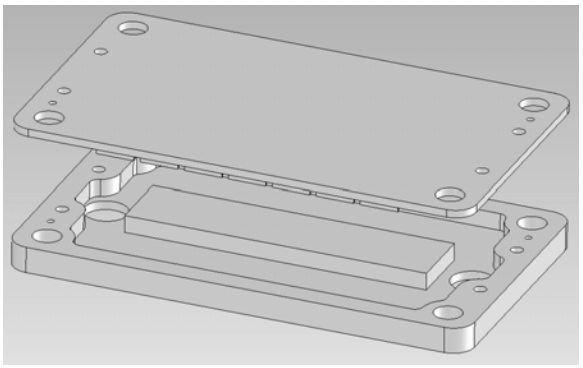

Figure 9 Heat sink design

DC TESTING

A basic DC characterization of the package was performed following the mounting of the plastic case. The DC evaluations were used to determine MOS-FET and diode current sharing and the module's thermal performance. The lid was removed during this testing and the devices were not potted to allow proper thermal imaging. The module was coated with spray boron nitride to provide the infrared (IR) camera with a consistent emissivity. The IR imaging system used provides ± 2 °C accuracy across the entire field of view enabling accurate assessments of device current sharing and health [8]. Lack of encapsulation limited the peak voltages requiring high power device condition to be extrapolated. During the testing the MOSFETs were biased with a 15 V gate-to-source voltage and the drain currents were analyzed from 0 - 400 A in 50 A increments. The power dissipation for each switch was determined by multiplying the current by the drain-to-source voltage. A separate test was used to measure the diode power dissipation that used a MOSFT gate-to-source bias of -10 V.

During DC testing the evaluation of thermal was accomplished using PGW 50/50 at inlet 30, 50, and 80 °C and flow rates of 1.9, 3.8, and 7.6 lpm. Figure 10 shows the upper switch and diode temperatures at 400 A with coolant conditions at 80 °C and 3.8 lpm. The device temperatures were cooler than

shown in

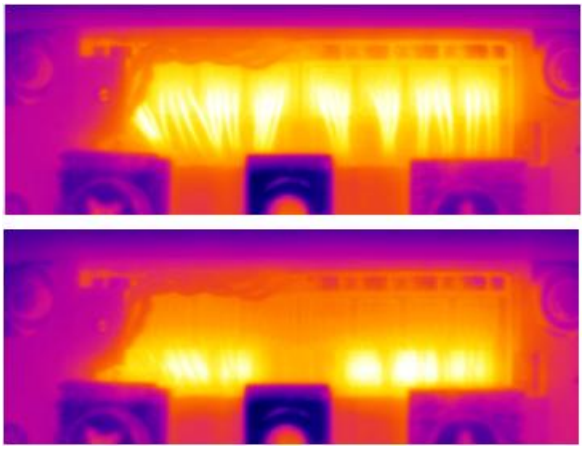

Figure 10 IR images at 400 DC using 80 ˚C coolant MOSFET (top), diodes (bottom)

due to the wire bonds requiring device temperatures to be sampled in areas away from the wire bonds.

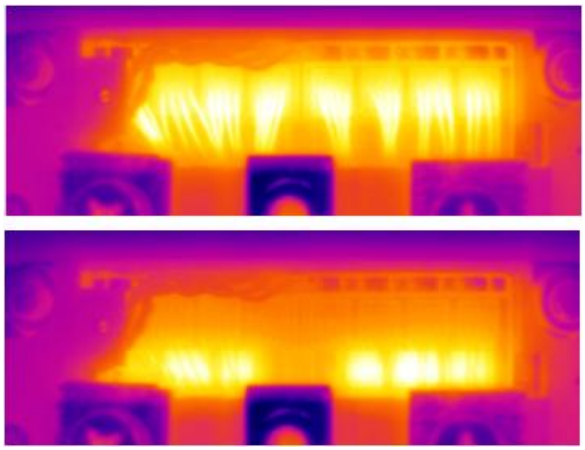

Figure 10 IR images at 400 DC using 80 ˚C coolant MOSFET (top), diodes (bottom)

The MOSFET die-to-die temperatures varied by only 3 °C indicating only a 2 A variation in die current at 50 A. Diode to diode temperature variation at an average die current of 67 A was 7 °C indicating an approximate 3 A die-to-die variation. Table 2 provides the power dissipation and thermal performance data for the upper switch and upper diode. Power dissipation is the total dissipated power in the conducting devices. ΔT_{AVG} is the average rise in die temperature. $R_\theta$is the normalized thermal resistance of the paralleled devices. The normalized thermal resistance provides a metric for comparing thermal resistances of systems having different thermal fluxes.

	Power Dissipation (W)	Inlet Coolant Temp. (˚C)	ΔT_{AVG} (˚C)	R_θ (˚C cm^2/W)
MOSFET	734	30	34	0.21
	711	50	31	0.20
	706	80	29	0.18
Diode	835	30	46	0.16
	906	50	49	0.16
	1036	80	53	0.15

Table 2 Experimental DC data of the upper switch and diode at 3.8 lpm coolant flow

AC TESTING

The module was tested under varying AC loads using ARL's DC-DC converter test bed. This test bed allows the testing of modules and devices using an open-loop boost converter design with a fixed resistive load of 4.5 Ω. The system allowed the module to be tested under 10, 15, 20, and 25 kW loads and varying switching frequencies from 10 to 30 kHz. For the testing described in this paper, the supply voltage was held at 100 V and the load voltages were varied from 209 V to 325 V. The maximum load voltage was limited to prevent inductive voltage swings from exceeding approximately 600 V during device turn-off. Figure 10 shows the IR image of the module during a short 27 kW test while switching at 20 kHz with 80 °C coolant.

The data obtained during the test run shown in Figure 11 was used to calculate the losses of the all SiC module and this data was compared with modeled results from a standard silicon IGBT module.

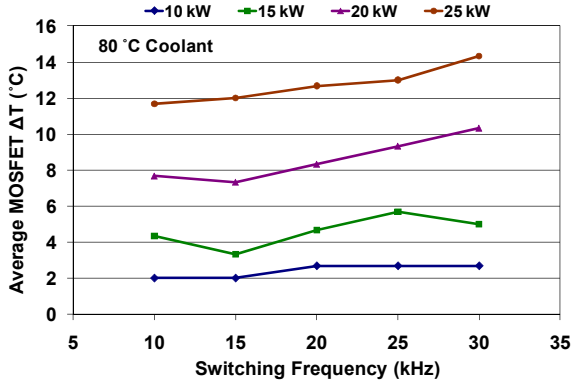

Figure 11 Average MOSFET temperature rise versus switching frequency for load power

Figure 12 shows that the conduction losses and total switching energies remain relatively constant in the MOSFET module. The minor increase in power dissipation in the MOSFET occurs from increased switching losses at the higher switching frequencies. This is stark contrast with the modeled IGBT modules results showing increased power dissipation 1 kW as switching frequency increases.

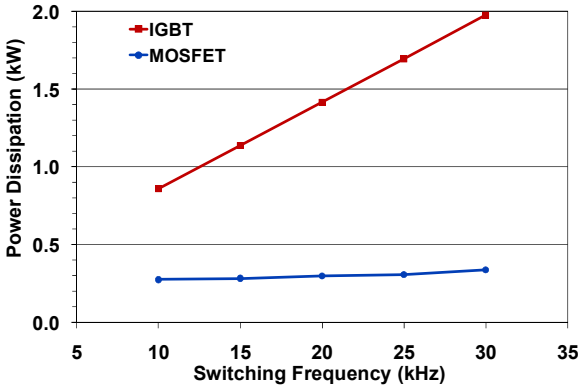

Figure 12 IGBT (simulated) versus MOSFET (experimental) power dissipation under 25 kW load

Comparison of the measured SiC diode to the modeled Si diode losses in Figure 13 showed a similar trend.

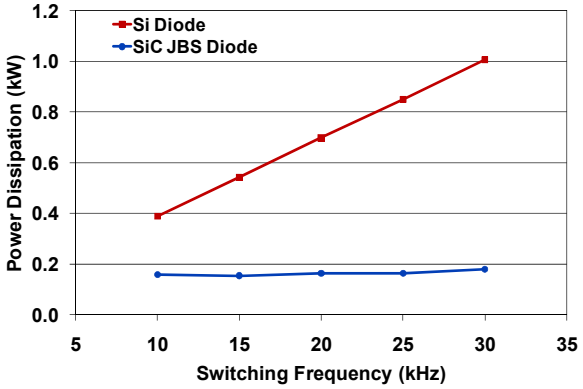

Figure 13 Si diode (simulated) versus SiC JBS diode (experimental) power dissipation under 25 kW load

The MOSFETs perform best at temperatures between 80 and 125 °C junction temperature (Table 3); therefore, operating at 100 °C coolant will cause increased losses.

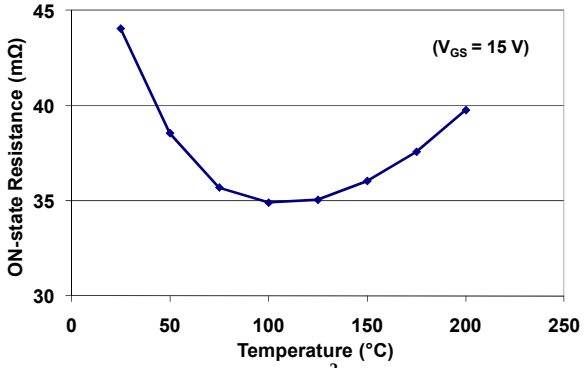

Table 3 Typical SiC 0.56 cm^2 MOSFET R_{DS-ON} vs. Temperature

Although the model predicts increased losses with 100 °C coolant, the SiC module would still outperform a silicon IGBT module in both losses and currant handling.

CONCLUSION

ARL has fabricated and tested a 1200 V, 400 A all SiC MOSFET module based on an industry standard form factor. The module was tested in ARL's DC-DC test bed under varying real-world loads and at differing frequencies. This is the first demonstration of an all SiC module of this size with varying AC loads. The results corroborated previous modeling that showed a dramatic reduction in losses over current silicon-based IGBTs. These results have demonstrated the feasibility of high temperature, high power switching with improved efficiency for a broad range of military and civilian applications.

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